UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,058	03/02/2004	Yoshinori Wakimoto	118755	9834

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/790,058	WAKIMOTO ET AL.
	Examiner	**Art Unit**	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2007*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4,6,8,10,12 and 15* is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4,6,8,10,12 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All   b)☐ Some * c)☐ None of:

         1.☐ Certified copies of the priority documents have been received.

         2.☐ Certified copies of the priority documents have been received in Application No. _____.

         3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed April 11, 2007

in response to the Office action dated November 11, 2007. Claims 2, 4, 10, and 12

have been amended. Claims 3 and 13-14 have been canceled. New claim 15 has

been added. Claims 2, 4, 6, 8, 10, 12, and 15 are pending in this application.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.   **Claims 2, 4, and 15 are rejected under 35 U.S.C. 103(a) as being obvious**

over Yoshizawa et al. (Patent Abstracts of Japan, "Associative Memory,"

Publication No. 2001-236790, published August 31, 2001) in view of Pereira et al.

(U.S. Patent 6,493,793) and Kanazawa et al. (U.S. Patent Application Publication

2002/122337).

3.   **As per claim 2**, Yoshizawa discloses a CAM device comprising:

a CAM array including a plurality of physical banks (paragraph 0011, lines 1-3;

Fig. 1, element 12); *It should be noted that "associative memory array" is analogous to*

"CAM array."

a logical bank-physical bank converter for setting the assignment between logical

banks and physical banks, and for outputting a control signal to set the configuration of

one or more physical banks assigned to the logical bank, depending on a logical bank

signal indicating a logical bank to be searched (paragraph 0012, lines 1-4; paragraph

0022, lines 1-4; Fig. 1, element 14); *It should be noted that "logic and physical signal*

transformation circuit" is analogous to "logical bank-physical bank converter", "logic

bank" is analogous to "logical bank", and "CONFIG <2:0>" is analogous to "control

signal to set the configuration of a physical bank assigned to the logical bank."

a priority circuit (paragraph 0015, lines 1-4; Fig. 1, element 16). *It should be*

noted that "priority network" is analogous to "priority circuit."

wherein in searching one of hit entries and empty entries,

i) if the CAM device includes one or more physicals banks assigned to the logical

banks to be searched:

the logical bank-physical bank converter outputs a search control signal to the

one or more physical banks so that each of the one or more physical banks output a

search result to the priority circuit (paragraphs 0041 and 0042). *It should be noted that*

the "SEARCH" signal is analogous to the "search control signal" and the "HIT" signal is

analogous to the "search result."

Yoshizawa does not expressly disclose a cascade circuit;

and the priority circuit outputs a search result of the CAM device depending on

the search result output from each of the one or more physical banks to the cascade

circuit;

and ii) if the CAM device includes no physical bank assigned to the logical bank

to be searched:

the logical bank-physical bank converter outputs a signal to the cascade circuit to

inform that there is no physical bank assigned to the logical bank so that the cascade

circuit generates one of a signal indicating that there is no hit entry in the CAM device

and a signal indicating that there is no empty entry in the CAM device as a search result

of the CAM device;

and the cascade circuit performs a logical operation on the search result of the

CAM device and a search result supplied from a higher order CAM device, and

transmits a result of the logical operation to a lower order CAM device.

Kanazawa discloses the priority circuit outputs a search result of the CAM device

depending on the search result output from each of the one or more physical banks

(paragraphs 0078-0079; Fig. 5);

and ii) if the CAM device includes no physical bank assigned to the logical bank

to be searched:

the logical bank-physical bank converter outputs a signal to inform that there is

no physical bank assigned to the logical bank (paragraphs 0080-0081; Figs. 5 and 6).

Yoshizawa and Kanazawa are analogous art because they are from the same

field of endeavor, that being cascaded content addressable memory.

At the time of the invention it would have been obvious to a person of ordinary

skill in the art to combine Kanazawa's shift circuitry with Yoshizawa's CAM array, logic

and physical signal transformation circuit, and priority circuit.

The motivation for doing so would have been to provide a spare CAM word as a redundant circuit without increasing a circuit scale and an output delay time, but rather improve product yield (Kanazawa, paragraph 0023, lines 4-6).

The combination of Yoshizawa/Kanazawa does not expressly disclose a cascade circuit;

and the priority circuit outputs a search result of the CAM device depending on the search result output from each of the one or more physical banks to the cascade circuit;

and ii) if the CAM device includes no physical bank assigned to the logical bank to be searched:

the logical bank-physical bank converter outputs a signal to the cascade circuit to inform that there is no physical bank assigned to the logical bank so that the cascade circuit generates one of a signal indicating that there is no hit entry in the CAM device and a signal indicating that there is no empty entry in the CAM device as a search result of the CAM device;

and the cascade circuit performs a logical operation on the search result of the CAM device and a search result supplied from a higher order CAM device, and transmits a result of the logical operation to a lower order CAM device.

Pereira discloses a cascade circuit generates one of a signal indicating that there is no hit entry in the CAM device and a signal indicating that there is no empty entry in the CAM device as a search result of the CAM device (col. 6, lines 18-25; Fig. 2, element 204);

and the cascade circuit performs a logical operation on the search result of the

CAM device and a search result supplied from a higher order CAM device, and

transmits a result of the logical operation to a lower order CAM device (col. 4, lines 48-

51; col. 4, line 63 – col. 5, line 1; col. 5, lines 59-60; col. 6, lines 18-25; Fig. 1, element

100; Fig. 2, elements 204 and 205). *It should be noted that "cascade logic circuit" is*

analogous to "cascade circuit", "match flag logic" is analogous to "priority circuit",

"/MFO" is analogous to "search results", "high-priority" is analogous to "high-order" and

"low-priority" is analogous to "low-order."

The combination of Yoshizawa/Kanazawa and Pereira are analogous art

because they are from the same field of endeavor, that being cascaded content

addressable memory.

At the time of the invention it would have been obvious to a person of ordinary

skill in the art to have Yoshizawa/Kanazawa's priority circuit output a search result of

the CAM device depending on the search result output from each of the one or more

physical banks to Pereira's cascade circuit as well as have Yoshizawa/Kanazawa's

logical bank-physical bank converter output a signal to Pereira's cascade circuit.

The motivation for doing so would have been to create a cascaded CAM array

with decreased time delay for match/hit flag generation.

Therefore, it would have been obvious to combine Yoshizawa, Kanazawa, and

Pereira for the benefit of obtaining the invention as specified in claim 2.

4.   **As per claim 4**, the combination of Yoshizawa/Kanazawa/Pereira discloses

when the searching is performed, the logical bank-physical bank converter outputs, to

each physical bank assigned to the logical bank to be searched, a control signal for

dynamically setting the configuration of the physical bank (Yoshizawa, paragraph 0030,

lines 1-3; Fig. 1). *It should be noted that "SRCH" is analogous to the "control signal for*

dynamically setting the configuration of the physical bank."

5.   **As per claim 15**, the combination of Yoshizawa/Kanazawa/Pereira discloses if

the CAM device includes no physical bank assigned to the logical bank to be searched,

the logical bank-physical bank converter outputs the signal directly to the cascade

circuit (Yoshizawa, paragraph 0045; Pereira, col. 6, lines 18-25; Fig. 2, element 204). *It*

should be noted that the with the combination of Yoshizawa/Kanazawa/Pereira

Yoshizawa's signal will be sent directly into Pereira's cascade circuit.

6.   **Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being obvious over**

Yoshizawa in view of Kanazawa and Pereira as applied to claims 2 and 4 above,

and in further view of Lyon (U.S. Patent 6,493,812).

7.   **As per claims 6 and 8**, the combination of Yoshizawa/Kanazawa/Pereira

discloses all the limitations of claims 6 and 8 except the logical bank-physical bank

converter is capable of assigning one physical bank to two or more different logical

banks.

        Lyon discloses the logical bank-physical bank converter is capable of assigning

one physical bank to two or more different logical banks (col. 2, lines 7-11). *It should be*

noted that "virtual" is analogous to "logical." It should also be noted that setting an

assignment between virtual banks to physical banks the real procedure that is taking

place is an assignment setting between the virtual and physical addresses of the banks.

The combination of Yoshizawa/Kanazawa/Pereira and Lyon are analogous art because they are from the same field of endeavor, that being addressing memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Lyon's virtual address aliasing technique within Yoshizawa/Kanazawa/Pereira's logic and physical signal transformation circuit.

The motivation for doing so would have been to increase memory performance by allowing cache data to be retained for multiple users and also access the cache data through different virtual addresses as the users change (Lyon, col. 7, lines 62-65).

Therefore, it would have been obvious to combine Yoshizawa/Kanazawa/Pereira and Lyon for the benefit of obtaining the invention as specified in claims 6 and 8.

8.   Claim 10 is rejected under 35 U.S.C. 103(a) as being obvious over Yoshizawa in view of Kanzawa and Pereira as applied to claim 2 above, and in further view of Khanna et al. (U.S. Patent 6,393,514).

9.   **As per claim 10**, the combination of Yoshizawa/Kanazawa/Pereira discloses all of the limitations of claim 10 except said cascade circuit performs logical OR operation when the cascaded circuit generates the signal indicating that there is no hit entry, and performs logical AND operation when the cascade circuit generates the signal indicating there is no empty entry.

Khanna discloses said cascade circuit performs logical OR operation when the cascaded circuit generates the signal indicating that there is no hit entry, and performs logical AND operation when the cascade circuit generates the signal indicating there is

no empty entry (col. 5, lines 35-43; col. 6, lines 41-45; Fig. 6, element 32; Fig. 7, element 64). *It should be noted that "match" is analogous to "hit." It should also be noted that the incorporated reference, Khanna (U.S. Patent 6,175,513), discloses an OR gate that inputs various multiple match flags and outputs an overall multiple match flag.*

The combination of Yoshizawa/Kanazawa/Pereira and Khanna are analogous art because they are from the same field of endeavor, that being content addressable memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Khanna's multiple match flag logic and full flag logic within Yoshizawa/Kanazawa/Pereira's cascade logic circuit.

The motivation for doing so would have been to decrease the time delay between write instructions which causes valid data to be written to the last available CAM row and assertion of the full flag (Khanna, col. 1, line 66 – col. 2, line 2).

Therefore, it would have been obvious to combine Yoshizawa/Kanazawa/Pereira and Khanna for the benefit of obtaining the invention as specified in claim 10.

10.   **Claim 12 is rejected under 35 U.S.C. 103(a) as being obvious over Yoshizawa in view of Kanzawa and Pereira as applied to claim 2 above, and further in view of Lyon as applied to claim 8 above, and in further view of Khanna.**

11.   **As per claim 12**, the combination of Yoshizawa/Kanazawa/Pereira/Lyon discloses all of the limitations of claim 12 except said cascade circuit performs logical OR operation when the cascaded circuit generates the signal indicating that there is no

hit entry, and performs logical AND operation when the cascade circuit generates the

signal indicating there is no empty entry.

Khanna discloses said cascade circuit performs logical OR operation when the

cascaded circuit generates the signal indicating that there is no hit entry, and performs

logical AND operation when the cascade circuit generates the signal indicating there is

no empty entry (col. 5, lines 35-43; col. 6, lines 41-45; Fig. 6, element 32; Fig. 7,

element 64). *It should be noted that "match" is analogous to "hit." It should also be*

noted that the incorporated reference, Khanna (U.S. Patent 6,175,513), discloses an

OR gate that inputs various multiple match flags and outputs an overall multiple match

flag.

The combination of Yoshizawa/Kanazawa/Pereira/Lyon and Khanna are

analogous art because they are from the same field of endeavor, that being content

addressable memory.

At the time of the invention it would have been obvious to a person of ordinary

skill in the art to implement Khanna's multiple match flag logic and full flag logic within

Yoshizawa/Kanazawa/Pereira/Lyon's cascade logic circuit.

The motivation for doing so would have been to decrease the time delay between

write instructions which causes valid data to be written to the last available CAM row

and assertion of the full flag (Khanna, col. 1, line 66 – col. 2, line 2).

Therefore, it would have been obvious to combine

Yoshizawa/Kanazawa/Pereira/Lyon and Khanna for the benefit of obtaining the

invention as specified in claim 12.

Response to Arguments

12.   Applicant's arguments filed April 11, 2007 with respect to **claims 2, 4, 6, 8, 10, 12, and 15** have been fully considered but they are not persuasive.

13.   With respect to Applicant's argument regarding independent claim 2, the Examiner respectfully disagrees and directs Applicant to the new rejection of claim 2 above. As seen in the rejection above, when combining Yoshizawa, Kanazawa, and Pereira in the manner described, the combination discloses the limitations of claim 2.

14.   As for Applicant's arguments with respect to the dependent claims the arguments rely on the allegation that the independent claim 2 is allowable and therefore for the same reasons the dependent claims are allowable. However, as addressed above, the independent claim 2 is not allowable, thus, Applicant's arguments with respect to the dependent claims are not persuasive.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 2, 4, 6, 8, 10, 12, and 15** have received a second action on the merits and are subject of a second action final.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Arpan Savla
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July 9, 2007

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